ECE271, Chapter 4 Reading Report

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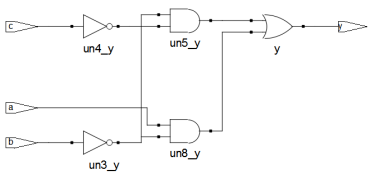
May 15th, 2017

This page demonstrates the expectation for doing examples for chapter 4.

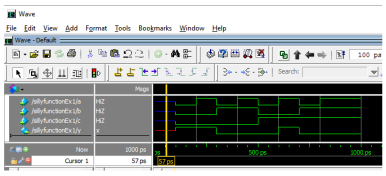
1 HDL Examples

```
1  module sillyfunction(
2      input logic a, b, c,
3      output logic y);
4
5  assign y = ~a & ~b & ~c
6           | a & ~b & ~c
7           | a & ~b & c;
8
9  endmodule
10
```

(a) System Verilog source



(b) SynplifyPro synthesis



(c) ModelSim simulation

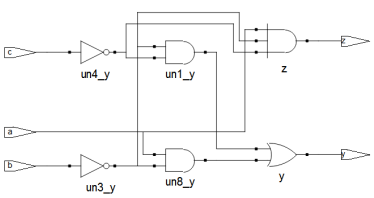
Figure 1: HDL Example 4.1

```
1  #Run the SillyFunction Example1 Simulation
2  add wave *
3  force a 0 @ 100, 1 @ 200, 0 @ 300, 1 @ 400, 0 @ 500, 1 @ 600, 0 @ 700, 1 @ 800
4  force b 0 @ 100, 1 @ 300, 0 @ 500, 1 @ 700
5  force c 0 @ 100, 1 @ 500
6
7  run 1000
8
```

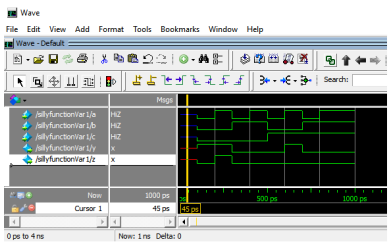
Figure 2: This do file can be used to simulate both example 4.1 and the variation within ModelSim.

```
1  module sillyfunction(
2      input logic a, b, c,
3      output logic y, z);
4
5  assign y = ~a & ~b & ~c
6           | a & ~b & ~c
7           | a & ~b & c;
8
9  assign z =  a & ~b & ~c
10          | a & ~b & ~c
11          | a & ~b & ~c;
12
13 endmodule
14
```

(a) System Verilog source



(b) SynplifyPro synthesis



(c) ModelSim simulation

Figure 3: Variation HDL Example 4.1